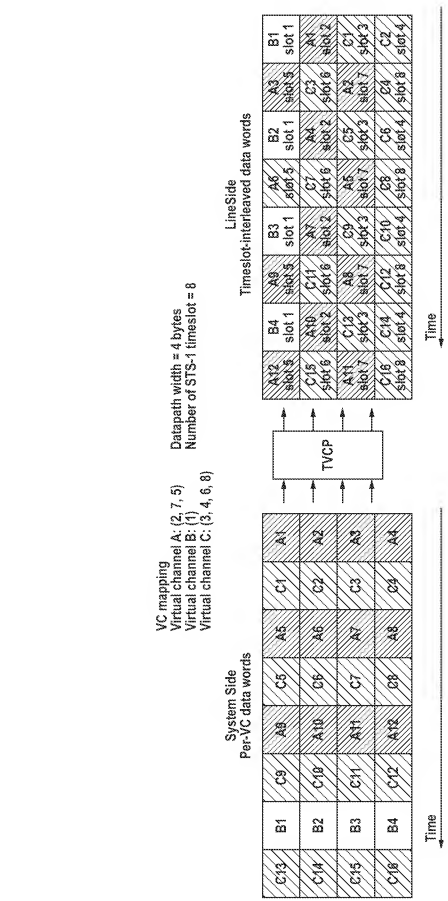
VC mapping
Virtual channel A: (2, 7, 5)
Virtual channel B: (1)
Virtual channel C: (3, 4, 6, 8)
Datapath width = 4 bytes
Number of STS-1 timeslot = 8
System Side
Per-VC data words
TVCP
LineSide
Timeslot-interleaved data words
Time
Time

FIG. 1

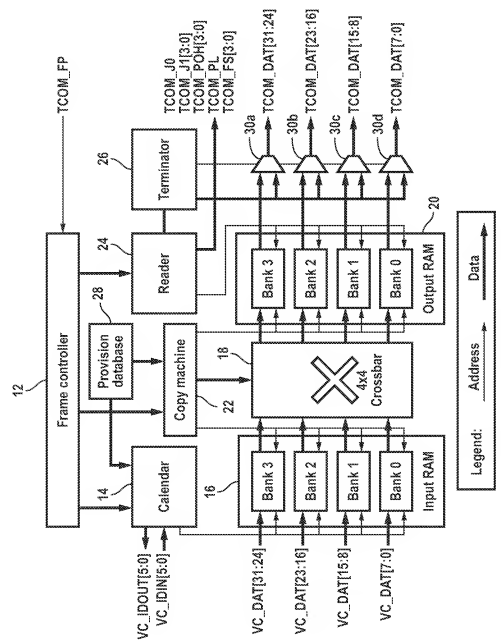
10
12
Frame controller
TCOM_FP
Provision database
28
Copy machine
22
Calendar
14
16
18
4x4 Crossbar
Reader
24
Terminator
26
TCOM_J0
TCOM_J1[3:0]
TCOM_POH[3:0]
TCOM_PS
TCOM_FS[3:0]
30a
30b
30c
30d
TCOM_DAT[31:24]
TCOM_DAT[23:16]
TCOM_DAT[15:8]
TCOM_DAT[7:0]
Bank 3
Bank 2
Bank 1
Bank 0
Output RAM
20
Input RAM
VC_IDOUT[5:0]
VC_IDIN[5:0]
VC_DAT[31:24]
VC_DAT[23:16]
VC_DAT[15:8]
VC_DAT[7:0]
Legend:
Address
Data

FIG. 2

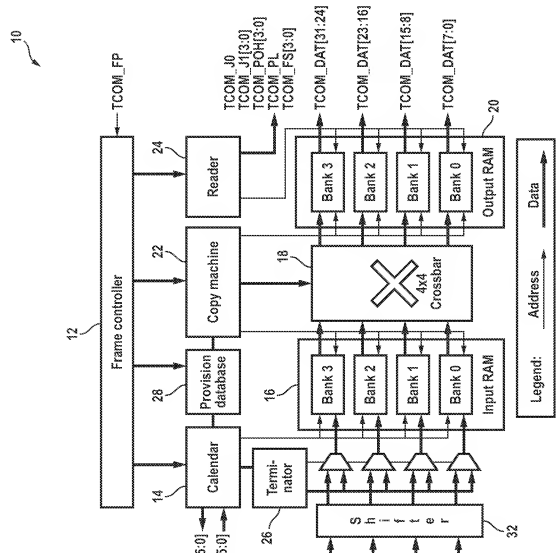
10
TCOM_FP
Frame controller
12
Reader
24
Copy machine
22
Provision database
28
Calendar
14
Termi-nator
26
Input RAM
16
Bank 3
Bank 2
Bank 1
Bank 0
18
4x4 Crossbar
Output RAM
20
Bank 3
Bank 2
Bank 1
Bank 0
TCOM_J0
TCOM_J1[3:0]
TCOM_POH[3:0]
TCOM_PL
TCOM_FS[3:0]
TCOM_DAT[31:24]
TCOM_DAT[23:16]
TCOM_DAT[15:8]
TCOM_DAT[7:0]
VC_IDOUT[5:0]
VC_IDIN[5:0]
VC_DAT[31:24]
VC_DAT[23:16]
VC_DAT[15:8]
VC_DAT[7:0]
Shifter
32
Legend:
Address
Data

FIG. 3

Channel	0	1		2		
Bandwidth	STS-1-1v	STS-1-2v		STS-1-3v		
Timeslot	4	1	5	3	0	2
Sequence Number	0	0	1	0	1	2

FIG. 4A

Timeslot	0	1	2	3	4	5
Channel	1	2	0	1	2	2
Sequence Number	1	0	2	0	0	1

FIG. 4B

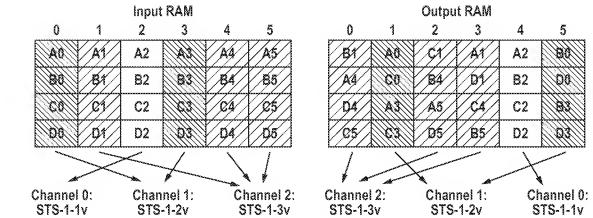

FIG. 4C

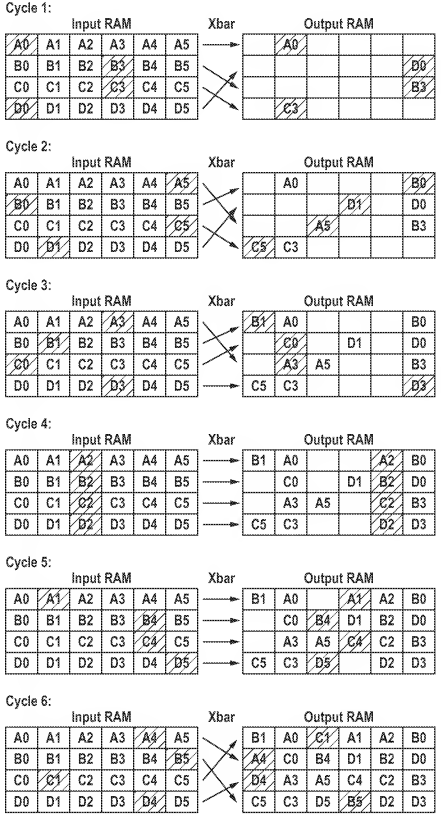
Cycle 1:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
A0
D0
B3
C3
Cycle 2:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
A0
B0
D1
D0
A5
B3
C5 C3
Cycle 3:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
B1 A0
B0
C0
D1
D0
A3 A5
B3
C5 C3
D3
Cycle 4:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
B1 A0
A2 B0
C0
D1 B2 D0
A3 A5
C2 B3
C5 C3
D2 D3
Cycle 5:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
B1 A0
A1 A2 B0
C0 B4 D1 B2 D0
A3 A5 C4 C2 B3
C5 C3 D5
D2 D3
Cycle 6:
Input RAM
Xbar
Output RAM
A0 A1 A2 A3 A4 A5
B0 B1 B2 B3 B4 B5
C0 C1 C2 C3 C4 C5
D0 D1 D2 D3 D4 D5
B1 A0 C1 A1 A2 B0
A4 C0 B4 D1 B2 D0
D4 A3 A5 C4 C2 B3
C5 C3 D5 B5 D2 D3

FIG. 5

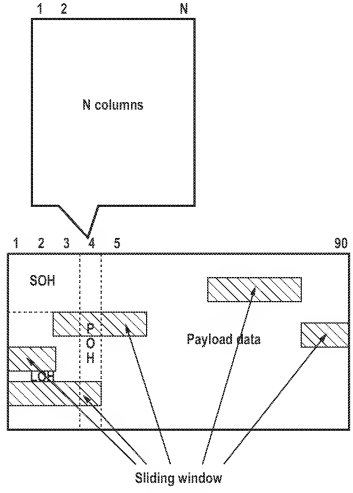

FIG. 6

Timeslot	1	2	3	4	5	6	7	8	9	10	11	12	1	2	...
STS-1	POH1	POH2	POH3	POH4	POH5	POH6	POH7	POH8	POH9	POH10	POH11	POH12	D1	D2	...
STS-3c	POH1	POH2	POH3	POH4	D1	D2	D3	D4	D1	D2	D3	D4	D1	D2	...
STS-12c	POH	FS	FS	FS	D	D	D	D	D	D	D	D	D	D	...
STS-24c	POH FS	FS FS	FS FS	FS FS	D D	D D	D D	D D	D D	D D	D D	D D	D D	D D	...
STS-36c	POH FS FS	FS FS FS	FS FS FS	FS FS FS	D D D	D D D	D D D	D D D	D D D	D D D	D D D	D D D	D D D	D D D	...
STS-48c	POH FS FS FS	FS FS FS FS	FS FS FS FS	FS FS FS FS	D D D D	D D D D	D D D D	D D D D	D D D D	D D D D	D D D D	D D D D	D D D D	D D D D	...

FIG. 7

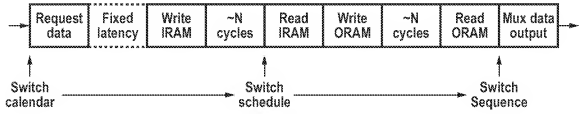

FIG. 8

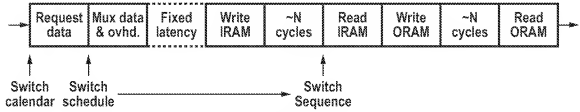

FIG. 9

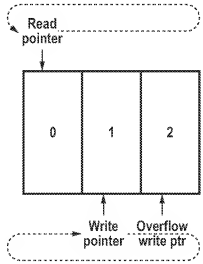

FIG. 10